ABSTRACT

The aim of the invention is to provide a speed control method for reducing current ripple and speed ripple at constant dynamics behavior while reducing the hardware required to a minimum. For this purpose, a control signal, especially a speed deviation (ev) is divided up into at least two signal portions (evhi and evlo). Every one of the at least two signal portions (evhi and evlo) is processed in a different manner. The low-order portion (evlo) can be smoothed by means of a low-pass filter (F). In an adder (Sum6) mounted downstream thereof, the differently processed signal portions are then added up for further control.